Claims

1. A semiconductor component (102, 202, 302), **characterized** in that the component comprises an electroconductive element (105, 205, 305) provided with at least one outlet (106, 206, 306), so that the electroconductive element (105, 205, 305) is groundable via an outlet (106, 206, 306) for shielding the semiconductor component (102, 202, 302) against electrostatic pulses.

2. A semiconductor component (102, 202, 302) according to claim 1, **characterized** in that in structure, the electroconductive element (105, 305) is a planar sheet.

3. A semiconductor component (102, 202, 302) according to claim 1, **characterized** in that the electroconductive element (105, 205) is a thin loop structure.

4. A semiconductor component (102, 202, 302) according to any of the preceding claims, **characterized** in that the electroconductive element (105, 205, 305) forms a permanent, integrated part of the semiconductor component (102, 202, 302).

5. A semiconductor component (102, 202, 302) according to claim 4, **characterized** in that the electroconductive element is placed underneath the cover element (104, 204, 304) of the semiconductor component (102, 202, 302), inside said cover element.

6. A semiconductor component (102, 202, 302) according to claim 4, **characterized** in that the electroconductive element is placed on top of the cover element (104, 204, 304) of the semiconductor component (102, 202, 302), outside said cover element.

7. A semiconductor component (102, 202, 302) according to any of the preceding claims, **characterized** in that the electroconductive element (105, 205, 305) is induced in the cover element (104, 204, 304) of the semiconductor component either chemically or electrochemically.

8. A method for shielding a semiconductor component (102, 202, 302) against electrostatic pulses, **characterized** in that in the semiconductor component (102, 202, 302), there is integrated an electroconductive element (105, 205, 305), and that for the integrated electroconductive element (105, 205, 305) there is provided

at least one outlet (106, 206, 306), so that the electroconductive element (105, 205, 305) is groundable through the outlet (106, 206, 306).

9. A method according to claim 8, **characterized** in that in the semiconductor component (102, 302), there is integrated an electroconductive, planar element.

10. A method according to claim 8, **characterized** in that in the semiconductor component (102, 202), there is integrated an electroconductive, loop-shaped element.

11. A method according to any of the preceding claims, **characterized** in that the electroconductive element (105, 205, 305) is integrated as a permanent part of the semiconductor component (102, 202, 302).

12. A method according to claim 11, **characterized** in that the electroconductive element is integrated underneath the cover element (104, 204, 304) of the semiconductor component (102, 202, 302), inside said cover element.

13. A method according to claim 11, **characterized** in that the electroconductive element is integrated on top of the cover element (204, 304) of the semiconductor component (102, 202, 302), outside said cover element.

14. A method according to any of the preceding claims, **characterized** in that the electroconductive element (105, 205, 305) is induced in the cover element (104, 204, 304) of the semiconductor component either chemically or electrochemically.

15. An apparatus including a mounting tray and components, **characterized** in that the device comprises a semiconductor component (102, 202, 302), in which there is integrated an electroconductive element (105, 205, 305), and where the electroconductive element is provided with at least one outlet (106, 206, 306) that is grounded to the ground plane of the mounting tray.